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A 10-BIT 10 GSPS OPTICAL ADC FOR RADAR SIGNAL PROCESSING

University of Connecticut

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13. ABSTRACT ***(Maximum 200 Words)***

Next generation radar systems for tactical aircraft will need to improve aircraft survivability, allow for cooperative multistatic mode of operation, provide efficient anti-jamming features, and compensate for motion-induced clutter. Faster digital processors are required, in particular analog-to-digital converters (ADCs) for digital processing of X-band radar systems. This effort investigated and demonstrated an optoelectronic scheme for a high-speed optical ADC. The system was designed with the following objectives in mind: a) maintain the RF signal in the electrical domain throughout the conversion process and eliminate use of bulky optical components; b) low optical power budget (e.g. basic sampling circuit requires 50-60 m optical power); c) direct interface to electronic quantization circuits; and d) compact design. The effort achieved sampling rates of 4 GSPS. The limitation in conversion speed was dictated by the photodiode which had a 3dB-bandwidth of 5GHz. The following tasks were completed: 1) Pspice simulation of sampling circuit; 2) Design implementation and synchronization of the optical clocks needed for a) sampling of incoming RF signals, b) demultiplexing the sampled signals to lower data rate for electronic quantization; 3) Interface of optical sampling circuit with National Instrument LABVIEW data acquisition system for quantization of sampled signals to produce an 8-bit gray code digital output; and 4) Optical sampling circuit optimization resulting in a 50% reduction in optical power consumption.

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A 10-bit 10 GSPS Optical ADC for Radar Signal Processing

Executive Summary

We investigated and demonstrated an optoelectronic scheme for a high-speed optical analog-to-digital converter. The system was designed with the following objectives in mind: a) to maintain the RF signal in the electrical domain throughout the conversion process and thereby eliminate the use of bulky optical components b) low optical power budget. For instance the basic sampling circuit require 50-60 μm optical power c) direct interface to electronic quantization circuits, d) compact design. In all a sampling rate of 4 GSPS was achieved. The limitation in conversion speed was dictated by the photodiode which had a 3dB-bandwidth of 5GHz. The following tasks were completed:

1) Pspice simulation of sampling circuit.

2) Design, implementation and synchronization of the optical clocks needed for a) sampling of incoming RF signals, b) demultiplexing the sampled signals to lower data rate for electronic quantization.

3) Interface of optical sampling circuit with National Instrument LABVIEW data acquisition system for quantization of sampled signals to produce an 8-bit gray code digital output.

4) Optical sampling circuit optimization resulting in a 50% reduction in optical power consumption.

1. PSPICE Simulation of optical Sampling Circuit

Figure 1 represents the basic optoelectronic RF sampling circuit. It consists of two back-to-back photodiodes arranged to act as a fast optoelectronic switch. The back-to-back arrangement is essentially an electrical open circuit, which can be taken to be the OFF-state of a fast optoelectronic switch. When the diodes are simultaneously actuated with a laser pulse, the switch toggles to the ON-state. Thus, a train of mode-locked laser pulses applied to the diodes of figure 1 will result in optical sampling of the RF input. The sampled RF appears across the load resistance.

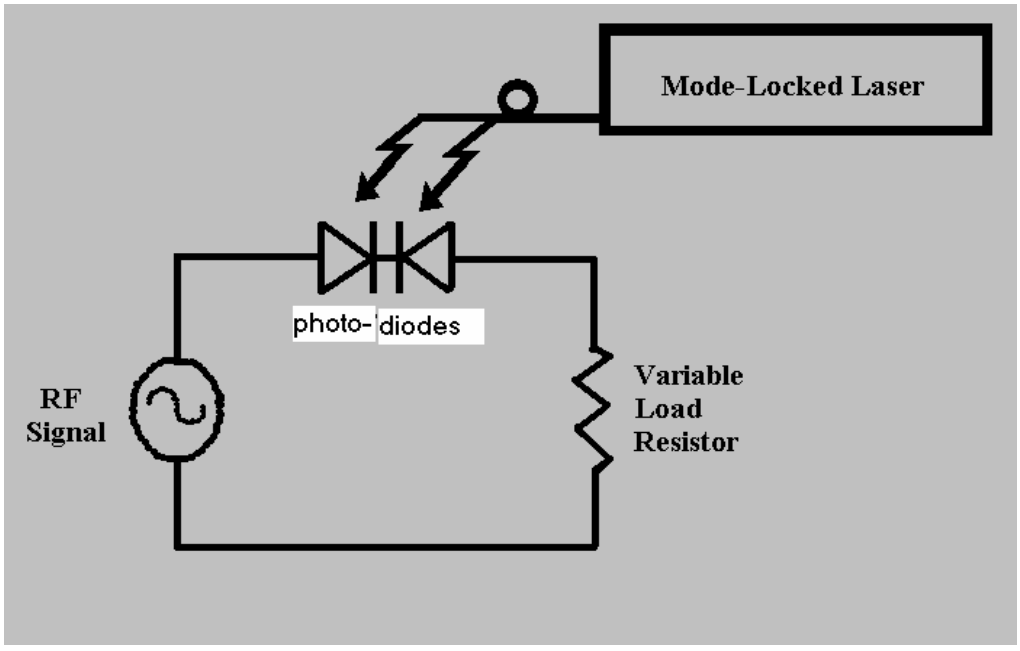


Figure 1. Basic RF sampling circuit. The circuit consists of two back-to-back photodiodes that act as fast optoelectronic switch actuated by mode-locked laser pulses.

A PSPICE circuit of figure 1 was designed and simulated. The diode was represented by its equivalent circuit, shown in figure 2. The ideal diode was represented in the PSPICE circuit as a switch, and the input optical pulses needed to actuate the switch were represented as electrical signal with the same repetition rate, amplitude and pulse-width as the laser pulses.

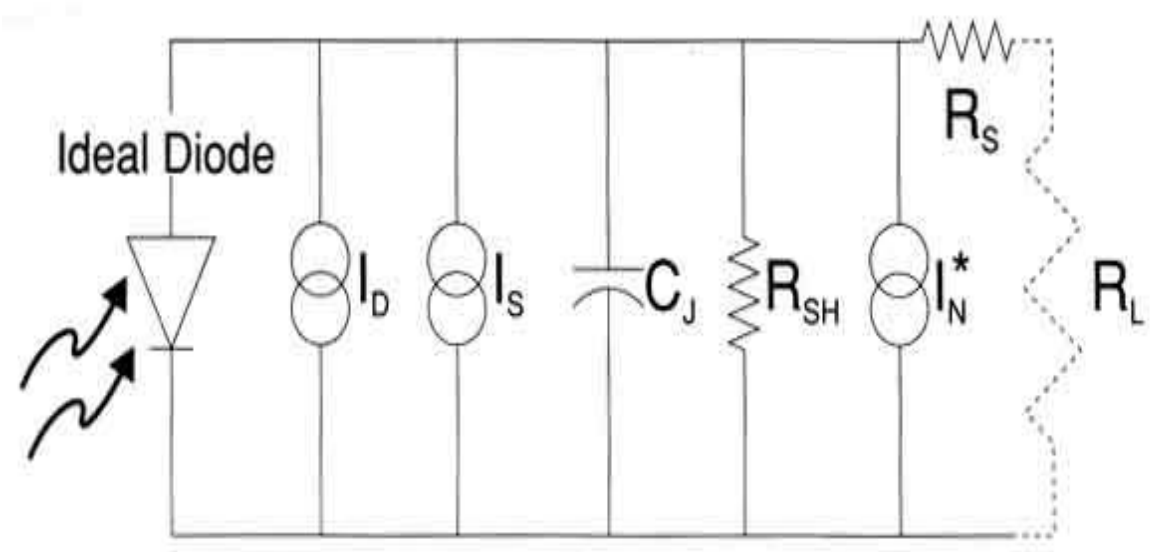


Figure 2. Equivalent circuit of photodiode.

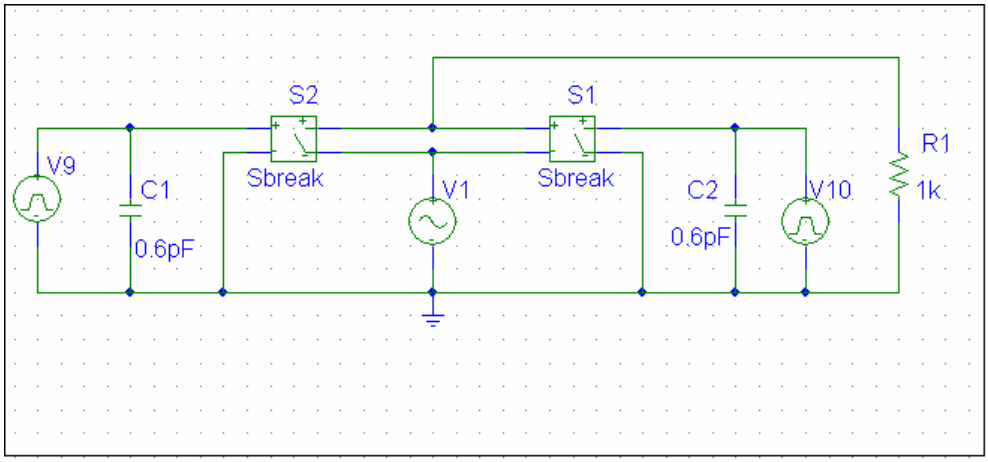


Fig. 3: PSPICE model for optoelectronic sampling circuit.

The parameter values for the components in figure 3 were obtained from manufacturers' data sheets for the photodiode. The "Sbreak" elements (S1 and S2) represent the optoelectronic switches in figure 1 (or the ideal diodes of figure 2).

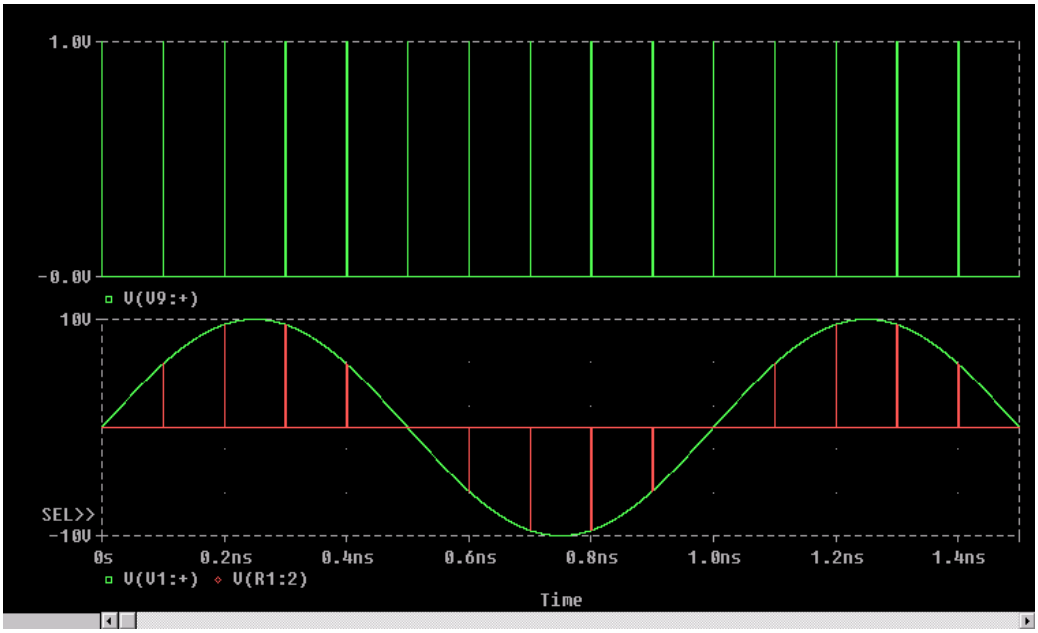


Figure 4. Simulation result for the sampling circuit. Top figure represents the sampling pulses, bottom figure represent the RF input and the sampled output.

A sample simulation is shown in figure 4. The upper graph depicts the pulses that actuate the photodiode. The input sinusoid and the sampled RF output are shown in the lower circuit.

2. Optical clock synchronization.

Two of the optical clocks required for the optical ADC system run at 1GHz and 250MHz respectively, and the third is digitally tunable between 10-100MHz. The 250MHz optical clock was tapped directly from the output of a 100ps 250MHz mode-

locked fiber laser. Tapping and circulating a portion of the 250MHz mode-locked laser output generated the 1GHz optical clock. The 1GHz and 250 MHz clocks are synchronized by virtue of the fact that they were generated from a single mode-locked laser source. The 10-100MHz tunable clock was generated from the output of a laser diode driven by an electronic laser driver circuit. The laser driver circuit is shown in figure 5. It is designed around an electronic counter chip MC100E136FN which takes as its input a sinusoidal signal and produces a digital output with a bit rate that is selectable between 10MHz and 100MHz. The output is taken from the Cout.

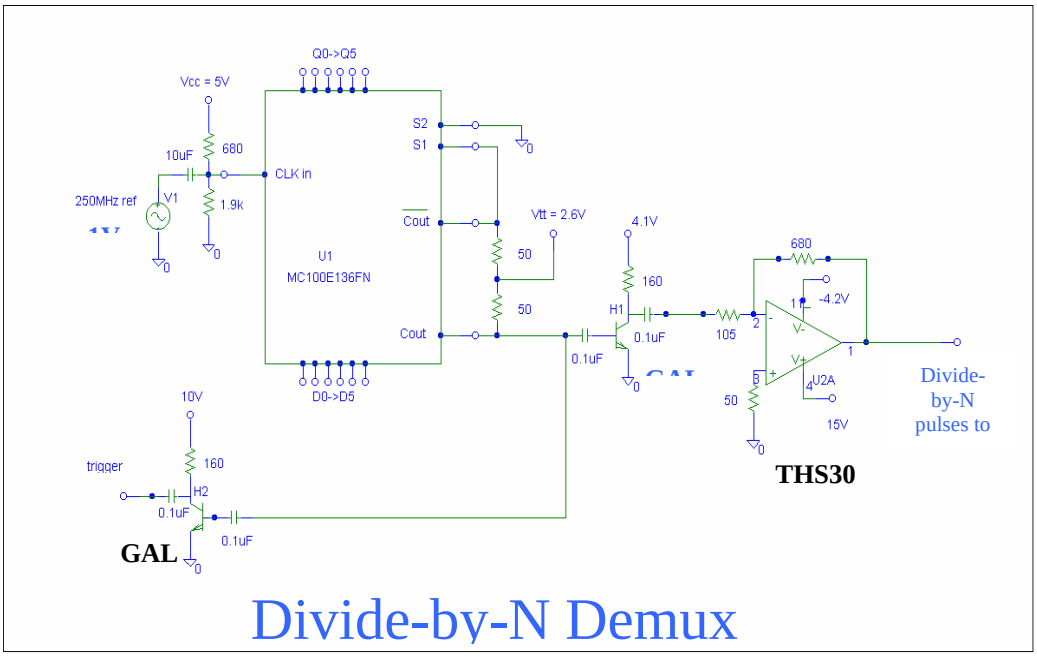


Figure 5. Electronic counter circuit used to drive a pigtailed laser diode. The laser diode output gives optical pulses 4ns wide and of variable repetition rate.

The frequency of the square wave depends on the setting of Q0-Q5 switches. The signal is amplified and buffered with the GAL-2 transistor circuits and the THS3001 chip. The

output of the counter circuit is used to drive a pig-tailed laser diode to produce an optical pulse width of 4ns. In order to synchronize the laser diode output signal with the other 1GHz and 250MHz clocks we tapped the 250 MHz RF signal needed to drive the input of the counter from the 250MHz reference signal of the mode-locked laser.

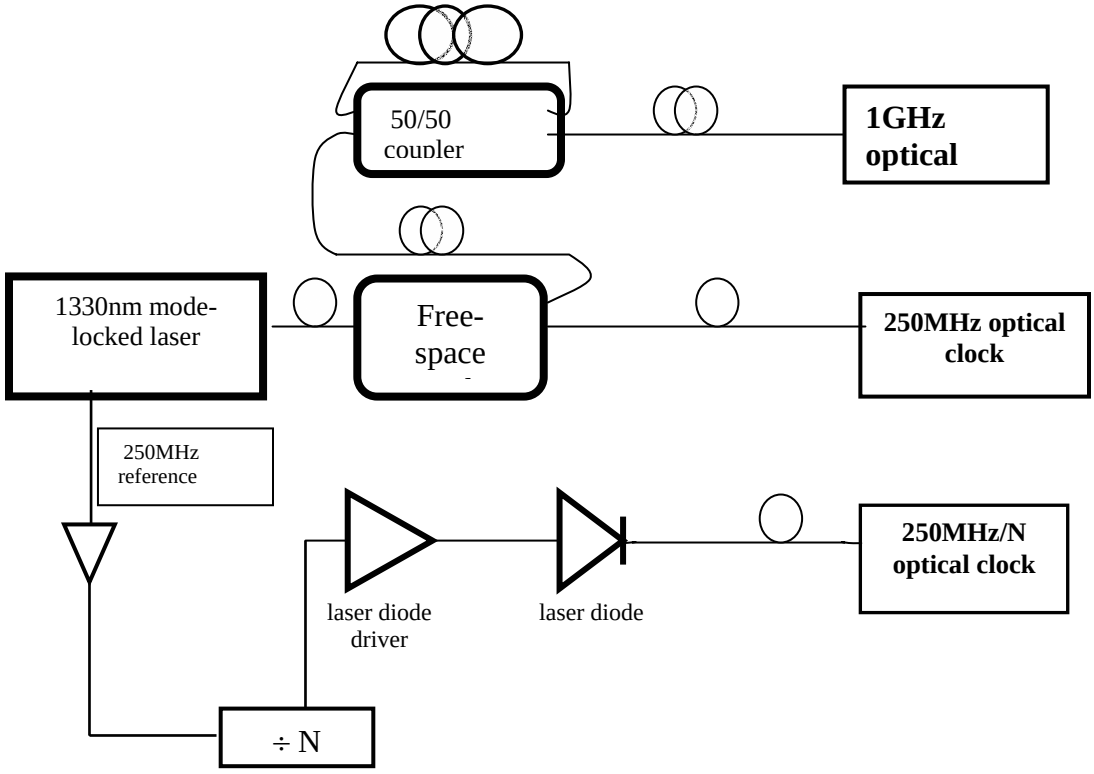


Fig. 6 Clock generation for sampling and demultiplexing

Fig. 6 shows a diagram representing the clock generation technique. The 250MHz (4ns rep rate, 100ps width at 1330nm) optical pulse from the mode locked laser serves as the clock for the intermediate tier of the sampling hierarchy. This optical pulse is then chosen to be 1.5 meters. A 250MHz sine wave reference (electrical) is available from the mode-locked laser. This reference is used as the standard from which the clock for the quantizing tier of the demultiplexing hardware is derived. An ECL counter set for

divide-by-N, where $\frac{250\text{MHz}}{\text{N}}$ is the maximum acceptable input rate of the selected quantizer, is used to demultiplex the 250MHz optical clock. This electrical signal is then used to drive a laser diode, which will control the photodiode. The width of the demultiplexed pulses are approximately 20ns wide, corresponding to the width of the demultiplexed optical pulses from the laser diode. Figure 7 is a high-speed digital display of the three clock pulses. The top is 25MHz, the middle 250MHZ, and the bottom 1GHz.

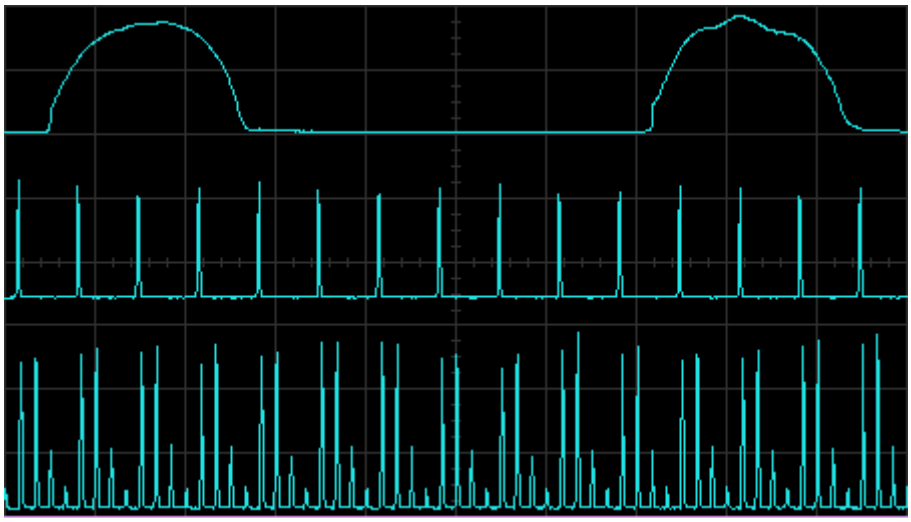


Figure 7 Oscilloscope display of Optical clock. Top is 25MHz, Middle 250MHz, bottom 1GHz.

3. Simulation of combined sampling/demultiplexing subsystem

Figure 8 shows the sampling circuit in the dashed block. The incoming 1GHz RF signal is amplified and split into multiple channels with each channel fed into a separate sampling circuit. The optical clock actuating the photodiodes has a repetition rate T = 1/f where f = 1 GHz. These clock pulses are sent via delay lines to the sampling circuits.

The delay lines are tailored so that each sampling circuit samples a different phase of the RF demultiplexing circuit.

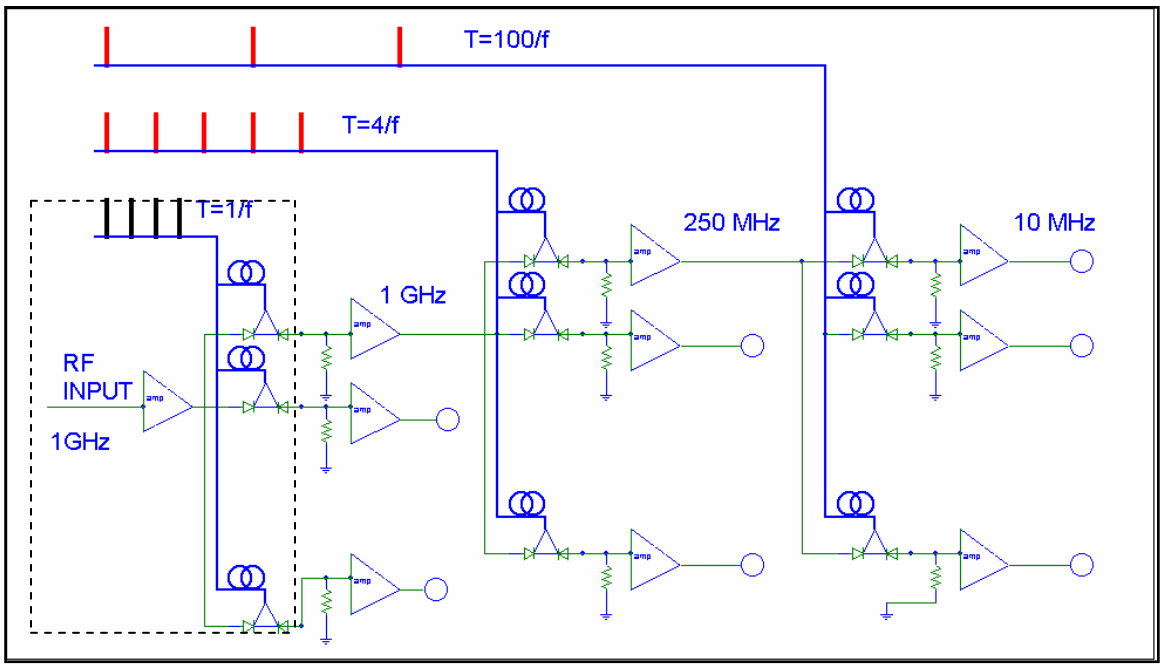


Fig. 8 PSPICE model for sampling block followed by demultiplexer blocks.

Figure 8 also shows a sampling circuit block followed by two demultiplexing blocks between successive stages. The demultiplexer circuit is similar to the sampling circuit. It is comprised of two back-to-back photodiodes, acting as fast optoelectronic switches that can be actuated by laser pulses. The first demultiplex circuit is actuated by 250 MHz clock pulses and the second by 25MHz clock pulses. As a result, the original 1GHz sampled RF pulses are demultiplexed into an aggregate of forty (40) 25-MHz sampled channels which can directly be quantized by electronic quantization circuitry. Once the data rate has been reduced considerably, electronic quantizers are then employed at the final stage of the optical ADC converter. A PSPICE model was designed and simulated for one of the forty channels. The SPICE model is shown in figure 9.

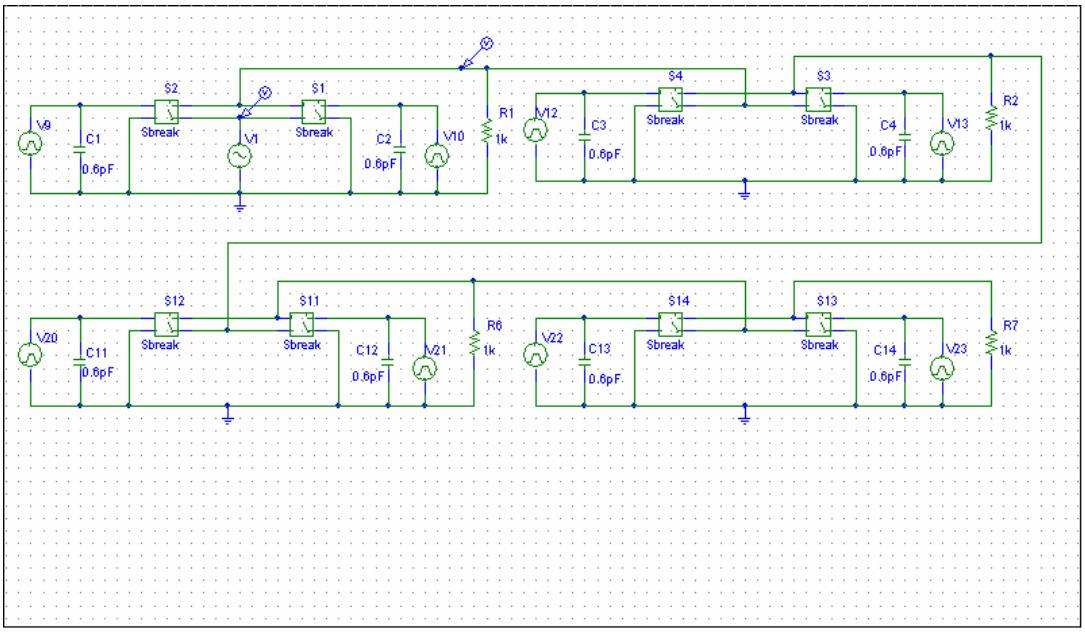


Figure 9. PSPICE model for the sampling/demultiplexer subsystem

Figure 10 is a simulation result for the sampling/demultiplexer subsystem. The top figure represents a 10 GHz pulse. The lower circuit represents the output of the sampling circuit. Notice that the sampling rate is 10GSPS. The middle figure represents one of the demultiplexed signals at a data rate of 1GSPS.

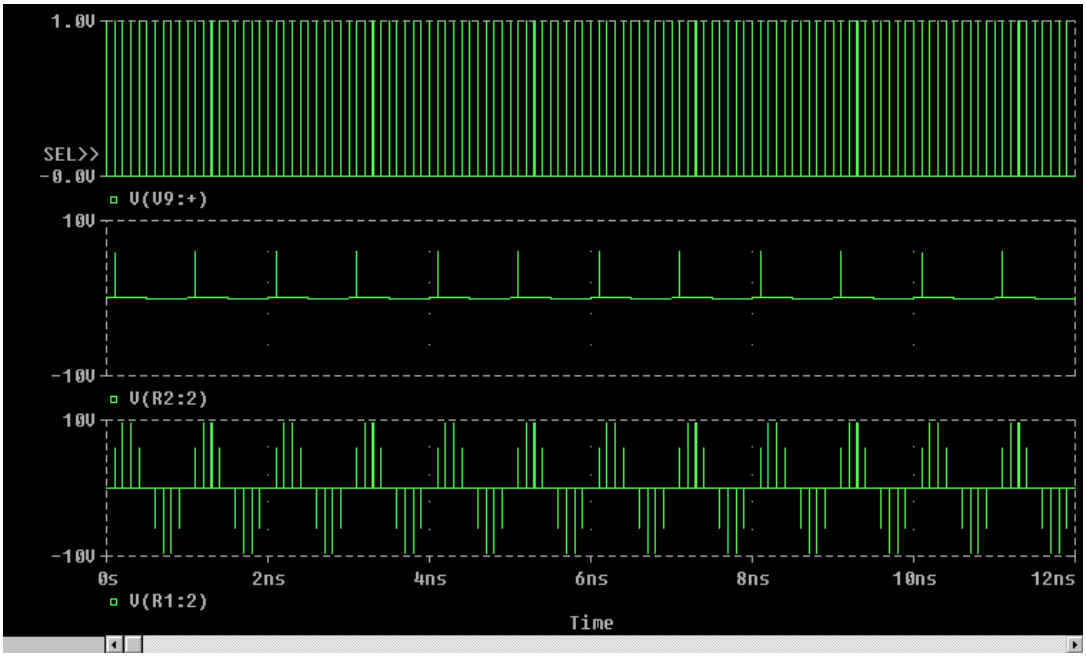


Figure 10. Simulation result for the circuit of figure 9. Top represents a 10 GHz pulse; middle represents one of the demultiplexed signals at data rate of 1GSPS; lower represents output of the sampling circuit at 10GSPS.

4. Quantization of sampled RF

For the quantization system a National Instrument LABVIEW hardware computer interface board was used. The output of the demux to the LABVIEW was connected to the scope input and appropriate Labview code was written to quantize the sampled signals. Figure 11 illustrates the front panel display of the LABVIEW-based quantizer. It represents the incoming sampled signals, and Figure 12 depicts the quantization levels of five of the sampled outputs. Both the analog amplitude and the corresponding gray code are displayed.

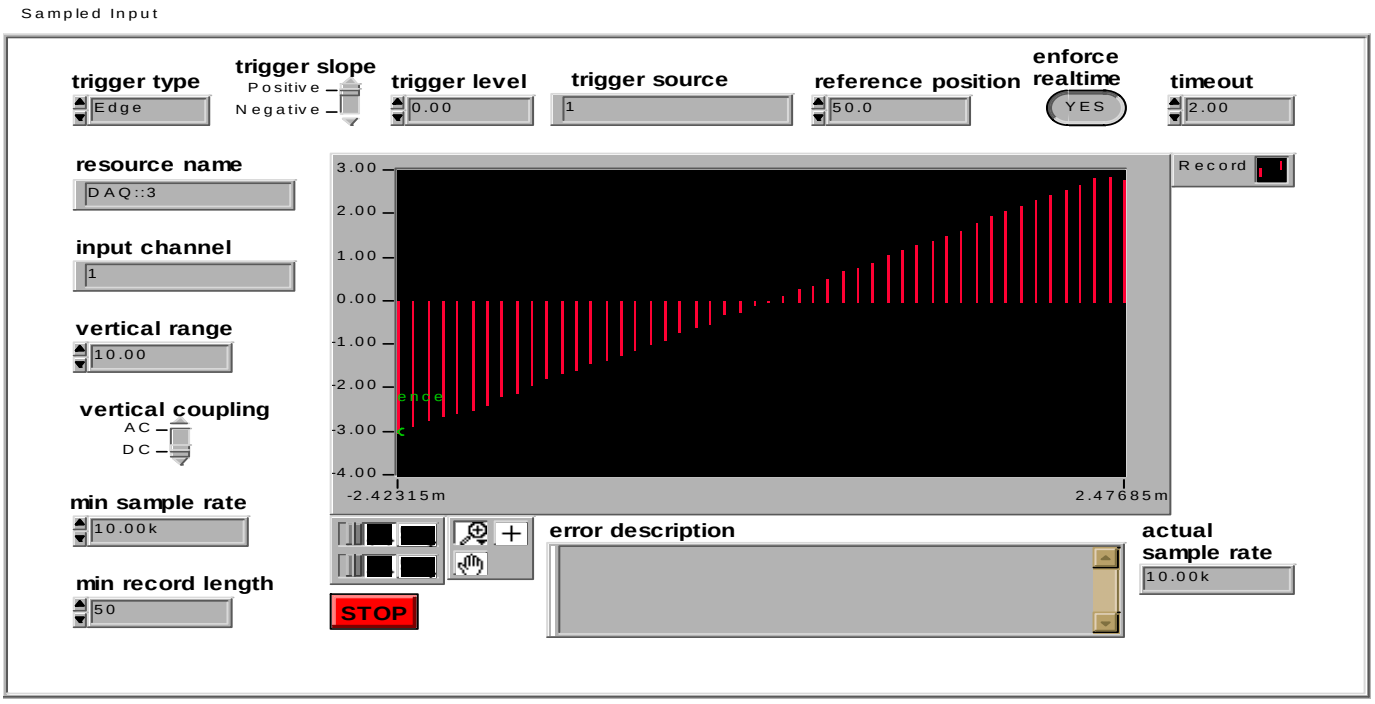


Fig.11 A portion of the sampled RF.

5. Discussion

Towards the end of the project it was demonstrated that a single photodiode can be T-biased to perform the same switching function similar to the back-to-back photodiode arrangement for RF sampling and demultiplexing. Figure 13a and Figure 13b show the original circuit and redesigned circuit respectively. The original design utilizes a back-to-back photodiode arrangement in the sampling circuit. The new design utilizes

only a single diode. However, to ensure that both positive and negative half-cycles of the input RF are sampled, a biased-T network is included.

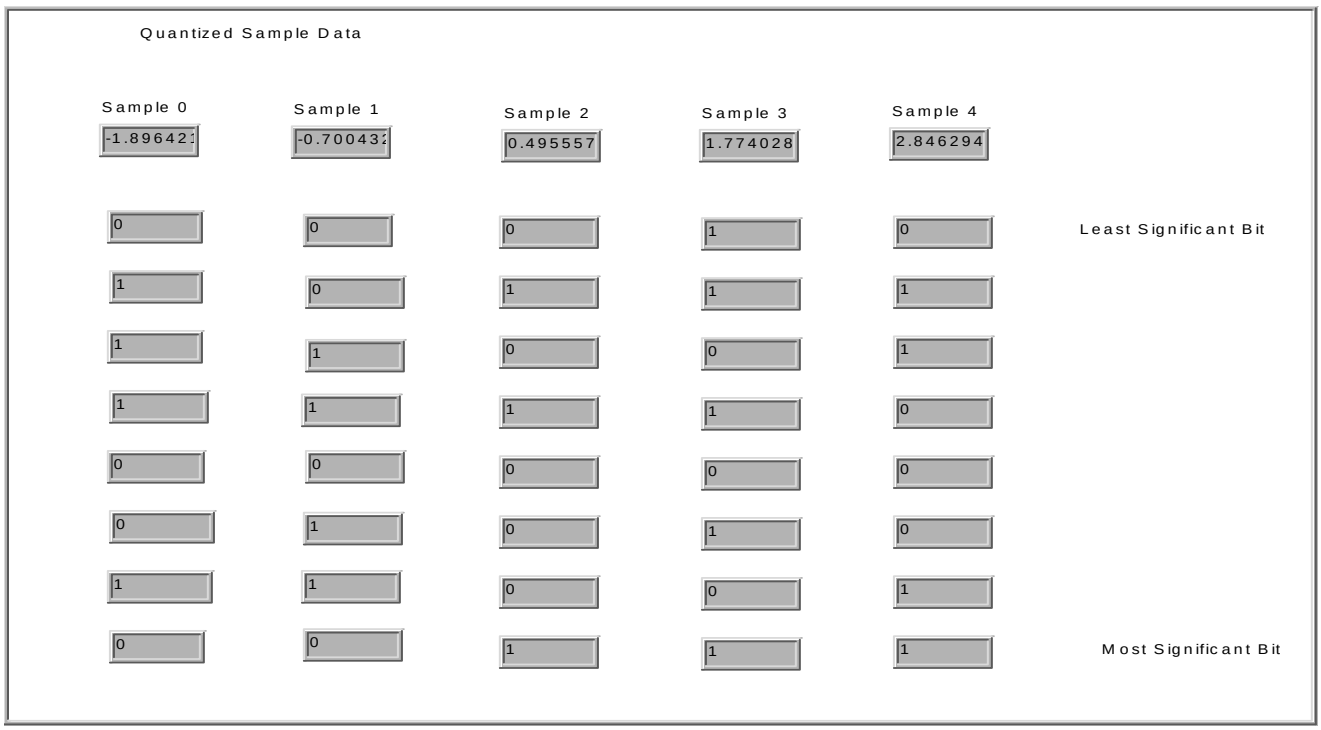
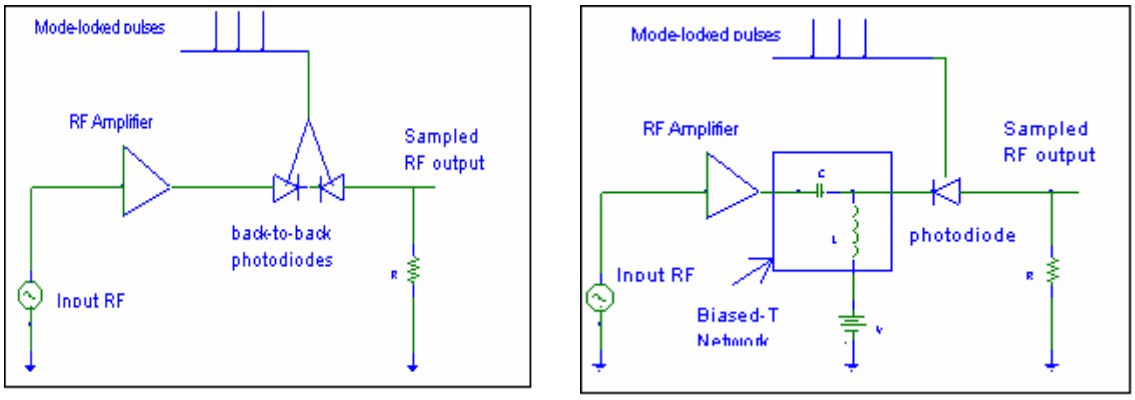


Figure 12. LABVIEW front panel display of the quantizer. The top panel shows incoming sampled data from the optical ADC into the Labview data board. The middle panel shows five of these sample data selected by Labview to quantize. The bottom panel shows the eight bit digital code for the quantized data.

The DC voltage is arranged to reverse bias the photodiode and its value is also chosen so that regardless of the RF amplitude the diode is always reverse biased. Under these conditions one the optical sampling pulses are applied. The sampled output rides over the DC voltage as reference.

The new design has many advantages. First, it utilizes only a single diode and requires 50% less optical power compared with the original circuit. Secondly, the

sensitivity of the diode is greatly enhanced when it is used in its reverse-biased configuration. Thirdly, it reduces the overall device count, and therefore lowers the cost and size of the complete optical ADC system.



(a) (b)

Figure 13. Original (a) and new-improved (b) optoelectronic sampling and demultiplexing circuit. The new design consumes 50% less optical power than the original design.